REMARKS

This amendment is being filed along with a Request for Continued Examination (RCE) application in response to the final Office Action having a mailing date of February 15, 2006. Claims 3-14, 16-20, and 23-24 are amended as shown. No new matter has been added. Claim 1 was previously canceled. With this amendment, claims 2-25 are pending in the application.

I. Preliminary Comments

In the final Office Action, the Examiner maintained his rejection of the claims primarily on the basis of Komoike (U.S. Patent No. 6,094,736) in combination with other references. Specifically, claims 2-5, 8-20 and 23 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Komoike in view of Kim et al. (U.S. Patent No. 6,148,426). Claims 24 and 25 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Komoike in view of Beauchesne (U.S. Patent No. 4,481,627). Claims 6, 7, 21 and 22 are rejected under 35 U.S.C. § 103(a) as being unpatenatable over Komoike in view of Kim and further in view of Rapoport (U.S. Patent No. 5,557,619).

The applicant is very appreciative of the Examiner's time and effort to provide the detailed analysis of Komoike in the final Office Action. Such detailed analysis has been helpful to allow the present applicant to further reconsider Komoike and the other references, and to formulate claim amendments that are believed to better distinguish the claims over the cited references.

The undersigned attorney would very much appreciate the opportunity to speak with the Examiner on the telephone, after the Examiner has had a chance to review this amendment. It is hoped that such a telephone conference would further assist the undersigned attorney in explaining the claim amendments in view of the cited references, and hopefully assist in helping move the application forward in a positive manner towards allowance. Therefore, if the Examiner's schedule permits and if the Examiner deems appropriate after initially reviewing this amendment, the Examiner is kindly requested to contact the undersigned attorney to arrange the telephone conference.

II. Rejections Under 35 U.S.C. § 112, Second Paragraph

In the final Office Action, claims 2-9 and 19-25 were rejected under 35 U.S.C. § 112, second paragraph, for being indefinite. Specifically, the Examiner stated that the "in a manner that" language in claims 20 and 23, the "as a" language in claims 7, 9, 19, 20, and 24, and the "is so" language in claim 7 were indefinite.

Accordingly, claims 20 and 23 are amended to address the indefiniteness rejection. Furthermore, claim 7 is amended to be definite and to include limitations consistent with its base independent claim 9.

It is respectfully submitted that the "as a" language in claims 7, 9, 19, 20, and 24 meet definiteness requirements. The limitations following this language (*e.g.*, "as a ROM" in claim 19) do form part of the claimed invention. For the basis in making the indefiniteness rejections with regards to the "as a" language, the Examiner has cited MPEP § 2173.05(d). However, this section of the MPEP discusses "such as" language (instead of "as a" language) that provides examples or preferences that should properly be set forth in the specification rather than in the claims.

The "as a" language in the referenced claims is clearly different from the "such as" language referred to in the MPEP, which are intended to list accompanying examples/preferences. In the referenced claims, the "as a" language provides a positive claim limitation that meets definiteness requirements. For example, the memory array behaving as a ROM in claim 19 clearly indicates that the memory has read-only (ROM) behavior, as compared to other kind of memory behavior such as random access memory (RAM) behavior.

Accordingly, the Examiner is kindly requested to withdraw the rejection of claims 7, 9, 19, 20, and 24 under 35 U.S.C. § 112, second paragraph.

III. Discussion of Applicant's Disclosed Embodiments

A disclosed embodiment will now be discussed in comparison to the applied references. Of course, the discussion of the disclosed embodiment, and the discussion of the differences between the disclosed embodiment and subject matter described in the applied references, do not define the scope or interpretation of any of the claims. Instead, such discussed

differences are intended to merely help the Examiner appreciate important claim distinctions discussed thereafter.

As discussed the previous amendment of December 8, 2005, an embodiment provided by the present applicants allow components (such as logic elements) of a semiconductor circuit to be tested, without having the problem of unpredictable contents of a memory influencing the test results of the logic elements. To accomplish this, one embodiment stores selected bit patterns in the memory, before testing the logic components, for the purpose of rendering the output of the memory predictable.

It is then possible to test the logic components directly connected to the output of the memory without having to worry about the memory behaving erratically. This is because the selected bit patterns are stored in the memory such that the output of the memory at any time is known and the memory can therefore be modeled by combinational logic and/or as a read-only memory (ROM). The logic components (separate from the memory) can then be tested using a test pattern without being influenced by unpredictable memory behavior. In an embodiment, the "selected" bit pattern is loaded to the memory before testing and a "test" pattern is used to test the logic components.

A few items can be noted from these embodiments. For instance, since the logic elements are directly connected to the output of the memory in one embodiment, the logic elements can receive the (predictable) output from the memory as part of and during the testing of the logic elements. Keeping the memory actively coupled to (or otherwise remained connected to) the logic elements during the testing of the logic elements allows the output from the memory to be used during the testing of the logic elements.

Such features are not disclosed, taught, or suggested by Komoike or any of the other cited references. For example in the final Office Action, the Examiner has provided a detailed explanation of the two (2) test processes used by Komoike to respectively test his DRAM 2 (memory) and then his CPU or a logic circuit 4. However, as will be explained below, these two test processes are distinct from one another, and do not keep the DRAM 2 actively coupled to the CPU and logic circuit 4 during the testing of the CPU and logic circuit 4, in a

manner that allows the output of the DRAM 2 to be used as part of the testing of the CPU and logic circuit 4.

Specifically, Figures 5A-5F of Komoike provides an explanation of his two testing processes to respectively test the DRAM 2 (memory) and the CPU and logic circuit 4. These testing processes can be summarized as follows:

Figures 5A-5B: a scan flip flop 9 having a flip flop 10 is shown. When the scan mode signal SM is in the high H level, a scan data signal SI is transferred to the flip flop 10. The H level corresponds to testing a circuit Y, which is the DRAM 2 (memory). When the scan mode signal SM is in the low L level, a data signal D is transferred to the flip flop 10. The L level corresponds to testing the circuit X, which is the CPU and logic circuit 4. The flip flop 10 outputs signals Q and QC, corresponding to D and SI, according to a clock signal T. *See, e.g.*, column 8, lines 24-34 of Komoike. The Q and QC outputs are connected to the circuit X and the circuit Y, respectively.

Figures 5C-5D: the scan mode is set to the H level to test the circuit Y (DRAM 2 or other memory test). The serial flip flops 9 each receive the SI data (shown as heavy solid lines in Figure 5C). The serial flip flops 9 then output parallel SI data to the circuit Y. The parallel output is shown in Figure 5D by the heavy solid lines from the flip flops 9 to the circuit Y. *See, e.g.*, column 8, lines 41 to 49 of Komoike. It is noted that column 8, line 49 of Komoike has a typographical error—the parallel output is shown in Figure 5D and not in Figure 5F.

Figure 5E: the scan mode is set to the L level to test the circuit X (the CPU and logic circuit 4). Data D is written into each of the flip flops 9 and transferred to the circuit X. *See, e.g.*, column 8, lines 51-55 of Komoike. The transfer of the data D is shown by the heavy solid lines in Figure 5E.

Figure 5F: next the scan mode is set to the H level, and output test data from the circuit X is transferred to the flip flops 9 and provided as scan output (SO) data items to an external device. *See, e.g.*, column 8, lines 56-62 of Komoike.

There are thus a few items that can be clearly noted from the summary above. First, the circuit Y and the circuit X are not actively coupled or otherwise remain connected to each other during the test of the circuit X in Figure 5E. Second, the circuit Y clearly does not

provide an output in Figure 5E that received by the circuit X and that is usable during or as part of the testing of circuit X in Figure 5E. Rather, the input of the circuit X during its testing is provided by the data D. Indeed, the fact that the outputs Q and QC of the flip flop 10 provide different types of data (SI and D) and are connected to different circuits X and Y, prevent the arrangement of Komoike from coupling the circuit Y to the circuit X (and/or to provide an output of the circuit Y to the circuit X) during the testing of the circuit X.

The other cited references do not cure the deficiencies of Komoike.

V. Discussion of the Claims

Independent claim 24 as previously presented is believed to be allowable over Komoike and the other cited references, whether singly or in combination. For example, claim 24 recited, *inter alia*, the feature of "receiving output from the memory array during the testing of the logic." As explained above, the circuit X of Komoike does not receive an output of the circuit Y during the testing of the circuit X in Figure 5E.

However, to facilitate prosecution, claim 24 is amended to recite "receiving output from the memory array as part of and during the testing of the logic." This amendment further clearly distinguishes claim 24 over Komoike and the other cited references, and therefore, claim 24 is further allowable.

Independent claim 20 has been amended to recite, *inter alia*, --said testing the logic including keeping the memory actively coupled to the logic during the testing of the logic to allow the output of the memory to be used during the testing of the logic--. As explained above, the circuit Y is not kept actively coupled to the circuit X during the testing of the circuit X in Figure 5E to allow the output of the circuit X to be used during the testing of the circuit X. Rather, the circuit X is provided with just the data D for testing and the circuit Y is decoupled or otherwise not actively coupled to the circuit X during the testing of the circuit X. Therefore, claim 20 is allowable over Komoike and the other cited references.

Independent claim 10 is amended to recite, *inter alia*, --the logic elements and the memory remain array actively coupled to each other during the test of the operation of the logic elements--. Its dependent claim 11 is amended to recite, *inter alia*, "connect the memory array

to the logic elements during the test of the operation of the logic elements." Dependent claim 19 recites, *inter alia*, that the memory has --an output that is usable during the test of the operation of the logic elements--. Komoike and none of the other cited references provide these features, as explained above. Therefore, these claims are allowable.

Independent claim 9 is amended to recite, inter alia, that the "combinational logic components and memory remain connected while testing the integrated circuit using the test pattern." The test pattern is further specified in claim 9 as being used to the combinational logic components. Because these features are not disclosed, taught, or suggested by any of the cited references, whether singly or in combination, claim 9 is allowable.

The various claims have been amended to provide proper antecedent basis, to more precisely recite the elements contained therein, or to otherwise place such claims in better form. Additionally, claims 12, 14, and 19 are amended to clarify that these claims and/or their related claims do not fall within the scope of 35 U.S.C. § 112, sixth paragraph.

IV. Conclusion

Overall, none of the references singly or in any motivated combination disclose, teach, or suggest what is recited in the independent claims. Thus, given the above amendments and accompanying remarks, the independent claims are now in condition for allowance. The dependent claims that depend directly or indirectly on these independent claims are likewise allowable based on at least the same reasons and based on the recitations contained in each dependent claim.

If the undersigned attorney has overlooked a teaching in any of the cited references that is relevant to the allowability of the claims, the Examiner is requested to specifically point out where such teaching may be found. Further, if there are any informalities or questions that can be addressed via telephone, the Examiner is encouraged to contact the undersigned attorney at (206) 622-4900.

The Director is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

All of the claims remaining in the application are now clearly allowable. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,

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